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APPLICATION NO.		FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO
09/927,457	•	08/13/2001	Laurent Fournier	FOURNIER=1	4159
1444	7590	05/23/2005		EXAMINER	
		EIMARK, P.L.L.C.	KENDALL, CHUCK O		
624 NINTH STREET, NW SUITE 300			ART UNIT	PAPER NUMBER	
WASHINGTON, DC 20001-5303				2192	
				DATE MAILED: 05/23/200	5

Please find below and/or attached an Office communication concerning this application or proceeding.

]							
•	Application No.	Applicant(s)					
	09/927,457	FOURNIER, LAURENT					
Office Action Summary	Examiner	Art Unit					
	Chuck Kendall	2192					
The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply							
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.  - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.  - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.  - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.  - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).							
Status							
<ol> <li>Responsive to communication(s) filed on 01/26/05.</li> <li>This action is FINAL. 2b)  This action is non-final.</li> <li>Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213.</li> </ol>							
Disposition of Claims							
4) ☐ Claim(s) 1-35 is/are pending in the application. 4a) Of the above claim(s) is/are withdrawn from consideration.  5) ☐ Claim(s) is/are allowed.  6) ☐ Claim(s) 1-35 is/are rejected.  7) ☐ Claim(s) is/are objected to.  8) ☐ Claim(s) are subject to restriction and/or election requirement.							
Application Papers							
<ul> <li>9) The specification is objected to by the Examiner.</li> <li>10) The drawing(s) filed on is/are: a) accepted or b) objected to by the Examiner.  Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).</li> <li>11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.</li> </ul>							
Priority under 35 U.S.C. § 119							
<ul> <li>12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).</li> <li>a) All b) Some * c) None of:</li> <li>1. Certified copies of the priority documents have been received.</li> <li>2. Certified copies of the priority documents have been received in Application No</li> <li>3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).</li> <li>* See the attached detailed Office action for a list of the certified copies not received.</li> </ul>							
Attachment(s)  1) Notice of References Cited (PTO-892) 2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date	4) Interview Summary Paper No(s)/Mail Da 5) Notice of Informal P 6) Other:						

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#### **DETAILED ACTION**

1. This action is in response to the application filed 01/26/05.

2. Claims 1 – 35 are pending.

### Claim Rejections - 35 USC § 103

- 3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
  - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 4. Claims 1 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bujanos USPN 5,572,664 in view of Brown III et al. USPN 5,450,555.

Regarding claims 1, Bujanos discloses, an apparatus for implementing a Floating-Point related application, comprising:

a tool that includes:

the language having set based constraints that facilitate defining Floating-Point events of interest in respect of at least one FP instruction (9: 27 - 42, see "C" language and double character);

- a parser for parsing the floating point commands (9: 20 25, see traverse);
- a processor configured to process at least the parsed commands for realizing the floating-point related application on the basis of said events (9:20 30).

Although Bujanos doesn't explicitly disclose receiving a list of floating point commands, Bujanos does disclose a floating point function unit (160) which executes floating point instruction sets (see FIG. 1, and associated text). Brown does disclose in

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an analogous art, receiving floating-point commands (11:25-35, see floating point unit). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Bujanos and Brown because, it would enable the floating point unit to be able to execute a wider range of floating point commands.

Regarding claim 2, the apparatus of claim 1, wherein said language further defining regrouping of the events into at least one coverage model; and

wherein said processor is configured to process the parsed commands for realizing the floating-point related application on the basis of said events and said at least one coverage model (Bujanos, 9:20 – 30).

Regarding claim 3, the apparatus according to claim 1, wherein said application is an evaluation of coverage of tests being run on a design (Bujanos, 11:25 – 35).

Regarding claim 4, the apparatus according to claim 1, wherein said processor is configured to generate a sequence of test vectors for verification of Floating-Point module operation (Bujanos,11:5 –15, see check tests test vectors);

the test vectors meet the constraints of said events (Bujanos, 2:32 – 36, see condition for constraints).

Regarding claim 5, the apparatus according to claim 4, wherein said verification includes verifying if the Floating-Point operation complies with IEEE standard for Floating-Point (Bujanos, 2:27 –32).

Regarding claim 6, for use with the Floating-Point module of claim 1, a computer language;

the language defining Floating-Point events of interest in respect of at least one FP instruction (5:5 - 7 for language see C++).

Regarding claim 7, the computer language of claim 6, further defining regrouping of the events into at least one coverage model (Bujanos, 7:48 – 65, see classify and grouping of instructions).

Regarding claim 8, which sites similarly to claim 1, see reasoning as previously discussed above.

Regarding claim 9, which sites similarly to claim 2, see reasoning as previously discussed above.

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Regarding claim 10, which sites similarly to claim 3, see reasoning as previously discussed above.

Regarding claim 11, which sites similarly to 5, see reasoning as previously discussed above.

Regarding claim 12, for use with the Floating-Point module of claim 8, a computer language;

the language defining Floating-Point events of interest and regrouping of events into at least one coverage model, in respect of at least one FP instruction, the coverage model having the form of a sequence of Floating-Point commands with constraints on (i) at least one intermediate result operand of the FP instruction, and (ii) result operand of the FP instruction (Bujanos, 9: 27 – 55, see "C"-language and double character);

Regarding claim 13, which sites similarly to claim 1, see reasoning as previously discussed above.

Regarding claim 14, which sites similarly to claim 3, see reasoning as previously discussed above.

Regarding claim 15, which sites similarly to claim 4, see reasoning as previously discussed above.

Regarding claim 16, which sites similarly to claim 5, see reasoning as previously discussed above.

Regarding claim 17, which sites similarly to claim 12, see reasoning as previously discussed above.

Regarding claim 18, the apparatus according to claim 1, wherein said list of commands includes:

range of FP numbers (Bujanos, 10:35 – 60);

mask on bits of FP number (Bujanos ,FIG. 9, 272, and associated text);

set or Reset Number of Bits in an FP number (Bujanos ,FIG. 9, 274, and associated text);

set or Reset Continuous-Bit-Long in an FP number (Bujanos ,FIG. 9, 270, and associated text);

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relative Values of at least two FP numbers, and logical operations among said Commands (Bujanos, 10:60-65).

Regarding claim 19, which sites similarly to claim 18 see reasoning as previously discussed above.

Regarding claim 20, which sites similarly to claim 18 see reasoning as previously discussed above.

Regarding claim 21, which sites similarly to claim 18 see reasoning as previously discussed above.

Regarding claim 22, which sites similarly to claim 18 see reasoning as previously discussed above.

Regarding claim 23, which sites similarly to claim 18, see reasoning as previously discussed above.

Regarding claim 24, which sites similarly to claim 18 above, see reasoning as previously discussed above.

Regarding claim 25, the apparatus according to claim 8, wherein said constraints are further applied to attributes of Machine State (Bujanos, 10: 1 – 10, for Machine state, see execution of requested FPU instruction using an assembly level instruction).

Regarding claim 26, the apparatus according to claim 25, wherein said constraints are further applied to attributes of Machine State (Bujanos, 10: 1 – 10, for Machine state, see execution of requested FPU instruction using an assembly level instruction).

Regarding claim 27, which is the method version of claim 1, see reasoning as previously discussed above.

Regarding claim 28, which is the method version of claim 8, see reasoning as previously discussed above.

Regarding claim 29, which sites similarly to claim 8, see reasoning as previously discussed above.

Regarding claim 30, which is the storage device version of claim 1, see reasoning as previously discussed above.

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Regarding claim 31, which is the program product version of claim 1, see reasoning as previously discussed above.

Regarding claim 32, which is the storage device version of claim 8, see reasoning as previously discussed above.

Regarding claim 33, which is the program product version of claim 8, see reasoning as previously discussed above.

Regarding claim 34, which is the machine readable version of claim 8, see reasoning as previously discussed above.

Regarding claim 35, which also cites similarly as claim 33 is the program product version of claim 8, see reasoning above as previously discussed.

## Response to Arguments

5. Applicant's arguments with respect to claims 1 - 35 have been considered but are moot in view of the new ground(s) of rejection.

#### Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

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the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chuck Kendall whose telephone number is 571-272-3698. The examiner can normally be reached on 10:00 am - 6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Dam can be reached on 571-272-3695. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ck.

SUPERVISORY PATENT EXAMINER

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